REMARKS

Claims 40, 49, and 84-93 have been canceled. Claims 39, 41-48, 50-56 and 74 have been amended. Marked-up versions of amended claims 39, 41-48, 50-56 and 74 are attached hereto as APPENDIX A. Claims 39, 41-48, 50-56 and 74 are pending in the application. Applicant reserves the right to pursue the original claims and other claims in this application and in other applications.

The Examiner objected to the specification. Per the Examiner's request, the specification has been amended to include the word "of" after the word "stoichiometry" on page 1, line 10. No new material has been introduced by this amendment. Accordingly, the objection should be withdrawn.

Claims 39 and 41-47 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Laibowitz et al., U.S. Patent No. 6,088,216 (hereinafter "Laibowitz"), in view of Azuma et al., U.S. Patent No. 5,516,363 (hereinafter "Azuma"). The rejection is respectfully traversed.

Claim 39 has been amended to clarify that a capacitor with improved BST dielectric sidewalls is being claimed. Claim 39 recites "[a] capacitor comprising: a material layer having . . . a sidewall region between . . . first and second levels; and an ion implantation doped BST high dielectric constant thin film material formed at least on said sidewall region." According to the claim, the doping of the BST high dielectric thin film material is such that the stoichiometry of said BST high dielectric thin film material is "substantially uniform at least at said sidewall region." Applicant respectfully submits that Laibowitz and Azuma do not teach or suggest the claimed invention.

Laibowitz discloses a DRAM capacitor comprising a substrate 12, whereupon a mesa 51 and high dielectric film 56 are formed (Figure 7). However, Laibowitz fails to teach or suggest a capacitor in which the stoichiometry of the sidewalls is substantially uniform. Additionally, Laibowitz fails to teach or suggest using BST as the dielectric layer.

It should be noted that Laibowitz discloses a thin film material deposition technique and resulting structure upon which the claimed invention improves upon.

Although Azuma discloses a DRAM circuit that uses a sputtering technique to layer its first electrode layer (Col. 17, line 62 to line 64), the Azuma reference fails to teach or suggest applying this method to a three-dimensional (3D) structure. In fact, the method taught by Azuma would not allow for sidewalls with improved stoichiometry on a capacitor with a 3D structure because it involves merely "dropping the precursor solution onto [a] substrate" (Col. 18, line 4 to line 5). The sidewalls in a 3D structure would not be covered if simple gravity were used to layer thin films onto the substrate as suggested by Azuma. In addition, the Azuma method requires that the substrate be spun "at about 1500 RPM (the preferred range is about 1500-2000 RPM) for about 30 seconds" after the depositing step (Col. 18, lines 5-8). This method could not be used on a 3D structure. Thus, the Azuma reference cannot be combined with the Laibowitz reference.

Furthermore, it should be noted that only the present application identifies and addresses the problem of maintaining the stoichiometry of the BST high dielectric constant thin film substantially uniform on the capacitor sidewall. Since none of the references recognize the problem, which is solved by the claimed invention, there is no motivation, teaching or suggestion in the references for the claimed invention. Indeed, the courts and PTO have uniformly established that recognition of the source of a problem renders a claimed invention unobvious. In re Sponnoble, 405 F.2d 578, 160 U.S.P.Q. 237 (C.C.P.A. 1969); Ex parte Campbell 211 U.S.P.Q. 575 (Bd. App. 1981). Stated otherwise, if the prior art does not even recognize the problem, the solution to the problem can not be deemed obvious. This is the situation here. Neither Azuma nor Laibowitz even recognize the problem addressed by the invention, much less teach or suggest its solution.

For at least the foregoing reasons, claim 39 is allowable over the combination of Laibowitz and Azuma. Claims 41-47 depend from claim 39 and are allowable along with claim 39. Accordingly the rejection should be withdrawn and the claims allowed.

Claims 48 and 50-56 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Laibowitz, in view of Azuma, and further in view of Leung et al., U.S. Patent No. 5,563,762 (hereinafter "Leung"). The rejection is respectfully traversed.

Claim 48 has been amended to recite "[a] capacitor comprising: a material layer having . . . a sidewall region between . . . first and second levels; an ion implantation doped BST high dielectric constant thin film material formed at least on said sidewall region; the doping of said BST thin film material being such that the stoichiometry of said BST high dielectric thin film material is substantially uniform at least at said sidewall region." A capping layer is also provided over at least a portion of said BST thin film material. Applicant respectfully submits that Laibowitz, Azuma and Leung do not disclose or suggest this structure.

As noted above with respect to claim 39, Laibowitz and Azuma fail to teach or suggest a doped BST thin film material at a sidewall region in which the stoichiometry at the sidewall region is substantially uniform. Leung discloses preparation of a capacitor whereby "a capping layer is deposited overall to encapsulate the capacitor structure" (Col. 2, line 46-49). Leung does not, however, disclose a capacitor with improved stoichiometry of the BST high dielectric constant thin film material on the capacitor sidewall. Accordingly, the combination of Laibowitz, Azuma and Leung fails to teach or suggest the subject matter defined in claim 48.

For at least the foregoing reasons, claim 48 is allowable over the combination of Laibowitz, Azuma, and Leung. Claims 50-56 depend from claim 48 and are allowable along with claim 48. Accordingly the rejection should be withdrawn and the claims allowed.

Claims 74-83 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Hosotani et al., U.S. Patent No. 6,051,859 (hereinafter "Hosotani") in view of Azuma. The rejection is respectfully traversed.

Claim 74 has been amended to recite an integrated circuit capacitor comprising "a . . . BST high dielectric constant thin film material" with "the doping of said BST high dielectric thin film material being such that the stoichiometry of said . . . material is substantially uniform at least at said sidewall region"

As noted above with respect to claims 39 and 48, Azuma fails to teach or suggest a doped BST thin film material at a sidewall region in which the stoichiometry at the sidewall region is substantially uniform. Although Hosotani teaches a capacitor comprising a substrate, first electrode, dielectric film, and second electrode, it does not teach or suggest an ion implantation doped BST thin film material as claimed. Accordingly the combination of Azuma and Hosotani fails to teach or suggest the subject matter defined in claim 74.

For at least the foregoing reasons, claim 74 is allowable over the combination of Azuma and Hosotani. Claims 75-83 depend from claim 74 and are allowable along with claim 74. Accordingly the rejection should be withdrawn and the claims allowed.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

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Respectfully submitted,

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APPENDIX A

Version With Markings to Show Changes Made

In the Specification:

The invention relates generally to ion implantation of high dielectric constant materials with dopants to improve the sidewall stoichiometry of high dielectric thin films deposited over 3-D formations. Particularly, the invention relates to ion implantation of Ti into a $(Ba,Sr)TiO_3$ (BST) film by varying the implantation angle of the dopant to improve the sidewall stoichiometry of the BST film. The invention also relates to integrated circuits having a doped thin film high dielectric material, used, for example, as an insulating layer in a capacitor.

In the Claims:

39. A [BST high dielectric constant thin film material having improved sidewall stoichiometry formed by the steps of] capacitor comprising:

[providing a substrate] a material layer having [at least one horizontal component and at least one vertical component] a first level and a second level, said first level and second levels being connected by a sidewall region between said first and second levels; and

[forming a] an ion implantation doped BST high dielectric constant thin film material [on said substrate;] formed at least at said sidewall region; [and]

the doping of said BST [high dielectric] thin film material [with a dopant by ion implantation, wherein said BST high dielectric thin film material is doped to] being

such that [maintain] the stoichiometry of said BST high dielectric thin film material is substantially uniform at least at said sidewall region.

41. The [BST high dielectric constant thin film material] capacitor according to claim [40] 39, wherein said dopants are selected from the group consisting of barium, strontium and titanium.

42. The [BST high dielectric constant thin film material] capacitor according to claim [40] 39, wherein said BST high dielectric thin film material is doped with a dopant selected from the group consisting of Ba[,] and Sr.

43. The [BST high dielectric constant thin film material] capacitor according to claim [40] 39, wherein said BST high dielectric thin film material is doped with Ti.

44. The [BST high dielectric constant thin film material] capacitor according to claim 43, wherein said doped BST high dielectric thin film material [is doped with Ti to maintain] contains a Ti percentage of from about 50% to about 53.5% throughout said BST high dielectric thin film material.

45. The [BST high dielectric constant thin film material] capacitor according to claim 44, wherein the ratio of Ba to Sr is about 70:30.

46. The [BST high dielectric constant thin film material] capacitor according to claim [40] 39, wherein said BST high dielectric thin film material is included in a DRAM cell.

47. The [BST high dielectric constant thin film material] capacitor according to claim [40] 39, wherein said BST high dielectric thin film material is formed [in] as part of a capacitor.

48. A [BST high dielectric constant thin film material having improved sidewall stoichiometry formed by the steps of] capacitor comprising:

[providing a substrate] a material layer having a first level and a second level, wherein said first level and second levels are connected by a sidewall region between said first and second levels;

[forming a] an ion implantation doped BST high dielectric constant thin film material [on said substrate] formed at least on said sidewall region; the doping of said BST thin film material being such that the stoichiometry of said BST high dielectric thin film material is substantially uniform at least at said sidewall region; and

[forming] a capping layer [over said first and second levels of said substrate;] provided over at least a portion of said BST thin film material.

[doping said BST high dielectric thin film material formed on said sidewalls of said substrate with a dopant by ion implantation, wherein said BST high dielectric thin film material is doped to maintain the stoichiometry of said BST high dielectric thin film material.]

50. The [BST high dielectric constant thin film material] capacitor according to claim [49] 48, wherein said dopants are selected from the group consisting of barium, strontium and titanium.

51. The [BST high dielectric constant thin film material] capacitor according to claim [49] 48, wherein said BST high dielectric thin film material is doped with a dopant selected from the group consisting of Ba[,] and Sr.

52. The [BST high dielectric constant thin film material] capacitor according to claim [49] 48, wherein said BST high dielectric thin film material is doped with Ti.

53. The [BST high dielectric constant thin film material] capacitor according to claim 52, wherein said doped BST high dielectric thin film material [is doped with Ti to maintain] contains a Ti percentage of from about 50% to about 53.5% throughout said BST high dielectric thin film material.

54. The [BST high dielectric constant thin film material] capacitor according to claim 53, wherein the ratio of Ba to Sr is about 70:30.

55. The [BST high dielectric constant thin film material] capacitor according to claim [49] 48, wherein said BST high dielectric thin film material is included in a DRAM cell

56. The [BST high dielectric constant thin film material] capacitor according to claim [49] 48, wherein said BST high dielectric thin film material is formed [in] as part of a capacitor.

74. An integrated circuit capacitor device comprising:

a [substrate] material layer having a first level and a second level, wherein said first and second levels are connected by a sidewall region between said first and second levels;

a first electrode provided [on said substrate] at least on said sidewall region;

a doped BST high dielectric constant thin film material provided on said first electrode, the doping of said [doped] BST high dielectric thin film material being [doped to maintain] such that the stoichiometry of said BST high dielectric thin film material is substantially uniform at least at said sidewall region; and

a second electrode provided on said BST high [capacitance] dielectric thin film layer [to complete said integrated circuit capacitor].